ISSN: 2277-9655
Scientific Journal Impact Factor: 3.449
(ISRA), Impact Factor: 1.852

IJESRT

INTERNATIONAL JOURNAL OF ENGINEERING SCIENCES & RESEARCH TECHNOLOGY

Design and Simulation of a High Performance Multiplier using Reversible Gates

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Abstract

Multipliers are the significant part of the present technology as they are mostly used in the convolution, fast Fourier transform, CPU designing etc. The speed and power dissipation of the multiplier operation is the very important factor. The reversible logic design provide the low power dissipation hence the multiplier designed using the reversible logic gates provide the low power dissipation and also the high performance. In our design we use the reversible logic gates are BVPPG gate, BME gate and MHNG gate. Our design provides high performance and also dissipates the low power than any other reversible design.

Keywords: Reversible logic circuits, Reversible logic gates, Reversible multiplier design, Partial product generator, Partial product adder.

Introduction

Irreversible hardware computation results in power dissipation due to information loss. As demonstrated by R. Landauer in the early 1960s, irreversible hardware computation, regardless of its realization technique, results in energy dissipation due to the information loss.

According to his research, the combinational logic circuits dissipate heat in an order of **kT ln2** joules of energy for every bit of information that is erased, where k is the Boltzmann constant and T is the operating temperature. For room temperature T the amount of dissipating heat is small (i.e. 2.9×10 - 21 joule), but not negligible. The reversible design does not dissipate heat and hence it is called so. In combinational logic heat dissipate due to the information loss. Such gates or circuits the inputs are equal to the outputs and we can determine the inputs from the outputs. Thus reversibility will become an essential property in future circuit design in terms of heat/power dissipation [1]. If a reversible gate has *k* inputs, and therefore *k* outputs, then we call it a k×k reversible gate. Any reversible circuit design includes only the gates that are reversible.

Reversible logic

The *n*-input *k*-output Boolean function f (*x1, x2… xn*) (referred to as (*n, k)* function) is called reversible if:

1) The number of outputs is equal to the number of inputs;
2) Each input pattern maps to a unique output pattern.

Reversible logic has applications in various research areas such as low power CMOS design, optical computing, quantum computing, bioinformatics, thermodynamic technology, DNA computing and nanotechnology. The difference of reversible logic synthesis compared to binary logic synthesis can be summarized as follows:

- The gates used to implement the circuit have the equal number of inputs and outputs.
- Every output of a gate, which is not used in the circuit, is a garbage signal.
- The total number of constants at inputs of the gates is kept as low as possible.
- A gate output can be used only once (the fan-out count of each output is equal to one). If two copies of a signal are required, a copying circuit is used.
- The resulting circuit is acyclic.

A reversible circuit should have the following features:

1) Design must use minimum number of reversible logic gates.
2) Design with minimum number of garbage outputs.
3) Design with minimum constant inputs.

Every output of a gate, which is not used for further computations, is a garbage signal.The input that is added to an nxk function to make it reversible

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Scientific Journal Impact Factor: 3.449
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is called constant input. In many computational units multiplication is a heavily used arithmetic operation. For the processors to have high speed multipliers is very important. In this paper, we present a reversible multiplier circuit using reversible MHNG gate. We demonstrate that the proposed reversible multiplier circuit is better than the existing Counter parts in terms of number of gates, number of garbage outputs, number of constant inputs and hardware complexity.

Reversible logic gates

An nxn reversible logic gate can be represented as:

$$Iv = (I1, I2, I2, \ldots, In)$$
$$Ov = (O1, O2, O3, \ldots, On)$$

Where Iv and Ov are input and output vectors respectively. Several reversible logic gates have been proposed in the past few decades. Some of them are: Feynman gate, Toffoli gate, Fredkin gate, Peres gate [1]. In this section we review these reversible logic gates. Some of them are presented to allow for comparison with existing studies.

Feynman gate (FG)

Feynman gate (FG), also known as controlled-not gate (1-CNOT), is a 2×2 gate that can be described by the equations:

$$Iv = (A, B)$$
$$Ov = (P = B, Q = A \oplus B)$$

where 'A' is control bit and 'B' is the data bit. It is shown in Fig. 1.

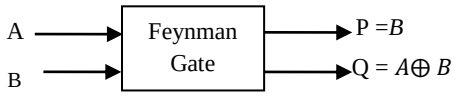

Fig 1: Feynman Gate.

Fredkin gate (FRG)

Fredkin gate (FRG), also known as controlled permutation gate, is a 3x3 reversible logic gate. It can be represented as:

$$Iv = (A, B, C)$$
$$Ov = (P = A, Q = A'B \oplus AC, R = A'C \oplus AB)$$

Where Iv and Ov are input and output vectors. It is shown in Fig. 2. Fredkin Gate is a conservative gate, that is, the Hamming weight of its input vector is the same as the Hamming weight of its output vector.

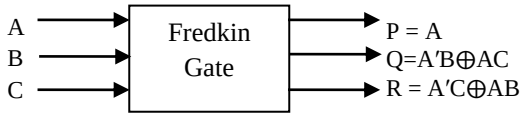

Fig 2: Fredkin Gate.

Toffoli gate (TG)

Toffoli gate (TG), also known as controlled controlled-not (CCNOT), is a 3x3 reversible logic gate. The Toffoli gate can be represented as:

$$Iv = (A, B, C)$$
$$Ov = (P = A, Q = B, R = AB \oplus C)$$

Where Iv and Ov are input and output vectors. The Toffoli gate is shown in Fig. 3.

Fig 3: Toffoli Gate.

Peres gate (PG)

Peres gate (PG), also known as New Toffoli Gate (NTG), combining Toffoli gate and Feynman gate is a 3x3 reversible logic gate. It can be represented as:

$$Iv = (A, B, C)$$
$$Ov = (P = A, Q = A \oplus B, R = AB \oplus C)$$

Where Iv and Ov are the input and output vectors. The Peres gate is shown in Fig. 4. Peres gate is equal with the transformation produced by a Toffoli Gate followed by a Feynman Gate.

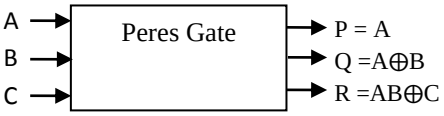

Fig 4: Peres Gate.

Reversible multiplier circuit

The operation of the 4x4 multiplier is depicted in Fig. 5. It consists of 16 partial product bits of the form xi,yi. The proposed reversible 4x4 multiplier circuit has two parts as follows.

1. Partial product Generator (PPG).
2. Partial Product Adder (PPA).

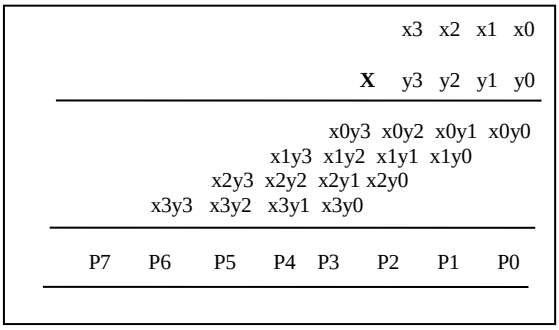

Fig 5: Operation Of The 4x4 Multiplier.

Partial Product Generator (PPG)

In PPG the partial products are generated in parallel. The reversible gates we used are BME gate

ISSN: 2277-9655
Scientific Journal Impact Factor: 3.449
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[2] and BVPPG gate [3]. The operation of the BVPPG and BME gate is depicted in Fig 6. Totally 8 Gates are used in PPG among them 6 are BVPPG and 2 are BME gates as the design shown in Fig 7. Total numbers of garbage outputs are 6 and constant inputs are 14.

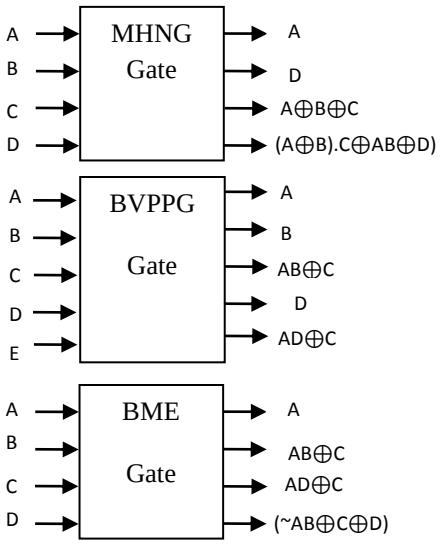

Fig 6: Reversible gates we used in this design.

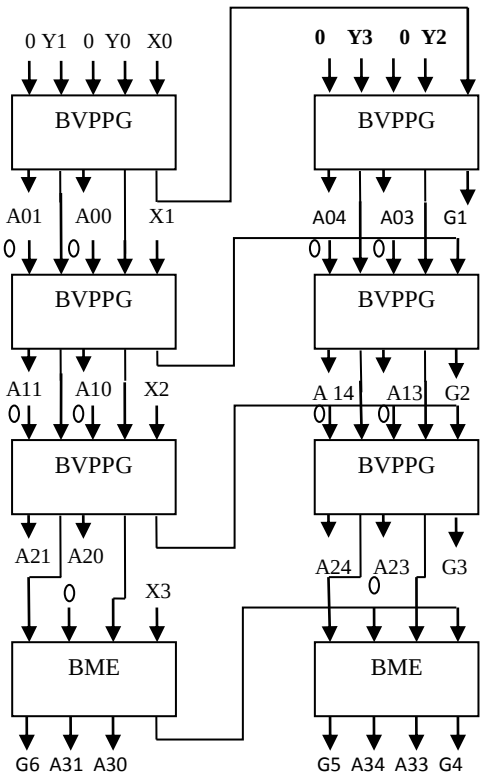

Fig 7: Partial Product Generator.

Partial Product Adder (PPA)

Partial Product Adder performs the addition of the partial products and to produce the final product of the input bits. The basic cells for the PPA are FULL adder and HALF adder. In PPA we use the reversible gates which perform the FULL adder and HALF adder operations. These operations are performed using the MHNG and Peres gates [4]. We have already come across with the Peres gate which generates SUM and CARRY in second and third output bits respectively. The operation of the MHNG gate in depicted in Fig 6.

One of the prominent functionalities of the MHNG gate is that it can work singly as a reversible full adder unit. If Iv = (A, B, Cin, 0), then the output vector becomes: Ov = (P=A, Q=0, R=Sum, S=Cout). Therefore, we have both of the required outputs. Implementation of the MHNG gate as the reversible full adder is shown in Fig 8.

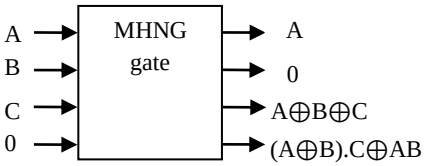

Fig 8: MHNG as full adder

We use the MHNG and Peres gates to construct the PPA. The proposed reversible multiplier circuit uses eight reversible MHNG full adders. In addition, it needs four reversible PERES half adders. The design of PPA is as shown in fig 9.(Fig 9 is shown at the end)

Result and analysis

The simulation result of the proposed reversible multiplier design is simulated in Verilog and resultimg wace pattern is shown in Fig 10. The proposed reversible multiplier circuit is more efficient than the existing circuit presented in [2-5]. Evaluation of proposed circuit can be comprehended easily with the help of the comparative results in Table 1. The difference between partial products generation design with the existing designs in [2-5] is the use of BVPPG gates and BME gates. This design method of partial product generation and the partial product adder has less hardware complexity. Therefore, the proposed reversible multiplier circuit is better than the existing

ISSN: 2277-9655
Scientific Journal Impact Factor: 3.449
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circuits in terms of complexity, number of garbage outputs and number of constant inputs. So, we can state that our design approach is better than all the existing counterparts in term of number of garbage outputs, constant inputs and no of gates used. From the above discussion we can conclude that the proposed reversible multiplier circuit is better than all the existing design.

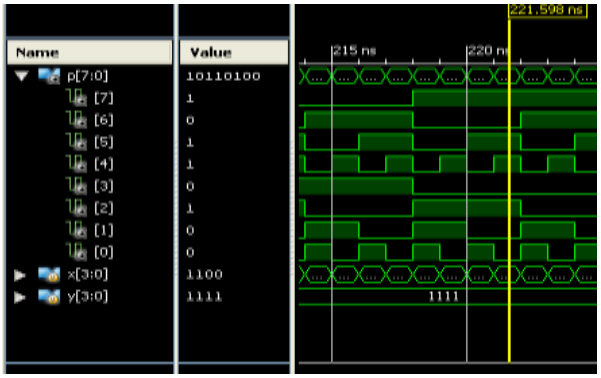

Fig 10: The simulation result of the proposed reversible multiplier design in verilog.

Table 1: Comparative Experimental Results of Different Reversible Multiplier circuits.

Paper no	*No of Garbage Outputs*	*No of Gates*	*No of Constant inputs*
This work	18	20	19
[4]	22	28	28
[2]	28	20	20
[3]	28	Not defined	Not defined
[5]	52	28	28

Conclusion

In this paper, we presented a 4x4 bit reversible multiplier circuit using reversible gates. Table 1 demonstrates that the proposed reversible multiplier circuit is better than the existing designs in terms of hardware complexity, number of logic gates, garbage outputs, and constant inputs. Our proposed reversible multiplier circuit can be applied to the design of complex systems in nanotechnology**.**

Acknowledgements

We would like to express our sincere thanks to head of the departaament Dr.Shantaram Rai and also we express our gratitude to our respective faculty Dept. of ECE,Canara Engineering, Banjanapadavu, Manglore and our parents, friends for supporting this work.

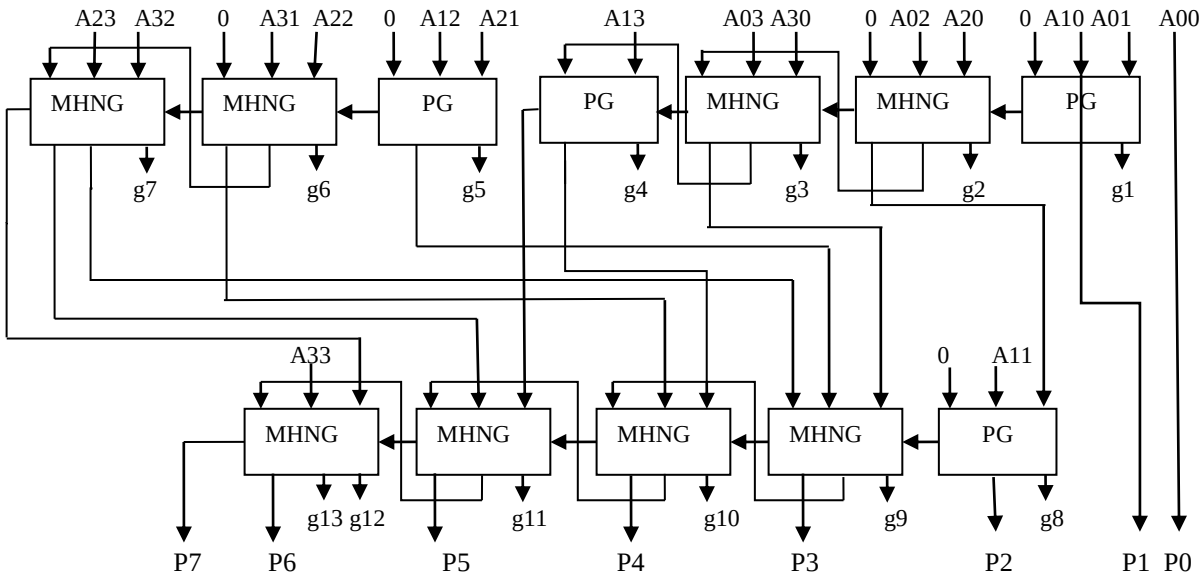

Fig 9: PPA using MHNG gates and Peres gates.

ISSN: 2277-9655
Scientific Journal Impact Factor: 3.449
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